(19) Europäisches Pat ntamt
European Patent Office
Office européen des brevets

(11) EP 1 132 819 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
12.09.2001 Bulletin 2001/37

(51) Int Cl.[7]: **G06F 13/16**, G06F 12/06

(21) Application number: **00311268.7**

(22) Date of filing: **15.12.2000**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **22.12.1999 GB 9930413**

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(54) Memory controller

(57) A memory controller for controlling the transfer of data to and from a memory array, wherein the memory array includes a first type of memory and a second type of memory, the first type having a different signalling protocol from the second type of memory, wherein the memory controller comprises:

an address decoder having an input for receiving a memory access request, said memory access request including the address of the memory array to be accessed, and an output for outputting the address of the memory array to be accessed;
a first sub-controller for generating a plurality of memory interface signals for controlling the first type of memory, said first sub-controller being operated in response to addresses within a first range of addresses output by the address decoder; and
a second sub-controller for generating a plurality of memory interface signals for controlling the second type of memory, said second sub-controller being operated in response to addresses within a second, non-overlapping range of addresses output by the address decoder.

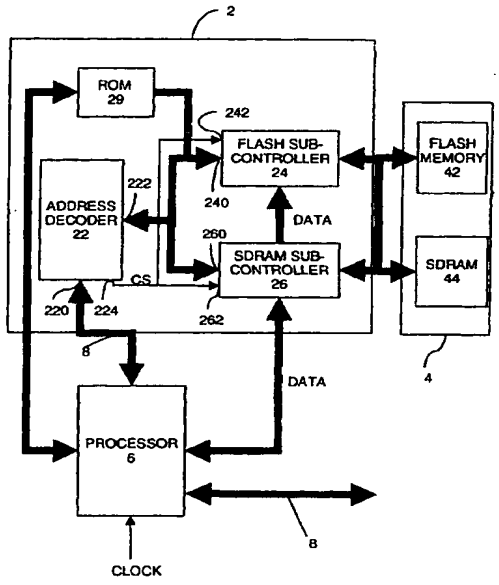

Fig. 1

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Description

[0001] This invention relates to a memory controller and in particular to a memory controller for controlling the transmission of data to and from a memory array comprising at least a first type and a second type of memory.

[0002] An example of a known memory controller is described in US Patent No. 5721860.

[0003] In accordance with the invention there is provided a memory controller for controlling the transfer of data to and from a memory array, wherein the memory array includes a first type of memory and a second type of memory, the first type having a different signalling protocol from the second type of memory, wherein the memory controller comprises:

an address decoder having an input for receiving a memory access request, said memory access request including the address of the memory array to be accessed, and an output for outputting the address of the memory array to be accessed;
a first sub-controller for generating a plurality of memory interface signals for controlling the first type of memory, said first sub-controller being operated in response to addresses within a first range of addresses output by the address decoder; and
a second sub-controller for generating a plurality of memory interface signals for controlling the second type of memory, said second sub-controller being operated in response to addresses within a second, non-overlapping range of addresses output by the address decoder.

[0004] A user can therefore define the areas of memory to be dedicated to a particular type of memory and add these types of memory as and when required. Such a memory controller therefore provides a user with the flexibility to connect different types of memory to a device via a single bus and to store information as to the address range to be allocated to a particular type of memory.

[0005] The memory controller of the invention may be used in a variety of electronic devices such as portable radio telecommunications devices (e.g. telephones and communicators).

[0006] Preferably the first type of memory is a burst mode type of memory, in particular flash memory. The memory may be synchronous or asynchronous. The addressing protocol may include multiplexed address and data.

[0007] Preferably parameters of the memory controller are configurable e.g. the first and second range of addresses may be configurable.

[0008] In accordance with the invention there is also provided a method of controlling the transfer of data to and from a memory array in an electronic device, wherein the memory array includes a first type of memory and a second type of memory, the first type having a different signalling protocol from the second type of memory, wherein the method comprises:

receiving a memory access request, said memory access request including the address of the memory array to be accessed, and outputting the address of the memory array to be accessed;
in response to addresses within a first range of addresses generating a plurality of memory interface signals for controlling the first type of memory; and
in response to addresses within a second, non-overlapping range of addresses generating a plurality of memory interface signals for controlling the second type of memory.

[0009] The invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

Figure 1 shows the components of a memory controller in accordance with the invention;
Figure 2 shows an example of the memory interface signals generated by a first sub-controller;
Figure 3 shows an example of the memory interface signals generated by a second sub-controller; and
Figure 4 shows an example of an implementation of a memory controller according to the invention.

[0010] As shown in Figure 1 a memory controller 2 in accordance with the invention comprises an address decoder 22 and at least a first sub-controller 24 and a second sub-controller 26. The memory controller 2 controls the transfer of data to and from a memory array 4 and operates under control of a microprocessor 6.

[0011] The memory array 4 comprises at least a first type of memory 42 and a second type of memory 44. The first type of memory 42 is of a burst mode type, preferably a synchronous burst mode type e.g. the flash memory chip 28F160F3 from Intel Corporation. The second memory type is a Synchronous Dynamic Random Access Memory (SDRAM). Generally software is stored in the SDRAM whilst it is not running in the burst mode memory. Generally the burst mode memory is used for the storage of code that is accessed frequently. Flash is the preferred type of burst mode memory since Flash memory is a non-volatile memory that can be erased in blocks. Flash is used to store application programs and user data and also provides "execute in place" functionality. Mask-ROM is another example of burst mode memory.

[0012] The memory controller 2 operates under control of a microprocessor 6, which may be dedicated to this task. However the microprocessor 6 may also be a microprocessor shared between many resources of the device with which the memory controller operates. The processor 6 is connected to the memory controller 2 via the internal system bus 8 of the ASIC of the device with

which the memory controller 2 is associated.

[0013] The microprocessor executes code that may be stored in the microprocessor itself or in the memory array 4. Thus the microprocessor has to access the memory array 4 via the memory controller 2 to transfer data to and from the memory array.

[0014] The address decoder has an input 220 for receiving a memory access request from the microprocessor 6. The memory access request includes the address of the memory array 4 to be accessed. The address decoder 22 has an output 222 for outputting the address to be accessed. The address decoder also has an output 224 for outputting a sub-controller select signal CS for selecting the sub-controller 24 or 26.

[0015] The first sub-controller 24 has an input 240 for receiving the address to be accessed and an input 242 for receiving the sub-controller select signal CS. In response to an appropriate CS signal the first sub-controller 24 generates a plurality of memory signals for controlling the Flash memory 42.

[0016] The second sub-controller 24 has an input 260 for receiving the address to be accessed and an input 262 for receiving the sub-controller select signal CS. In response to an appropriate CS signal the second sub-controller 24 generates a plurality of memory signals for controlling the SDRAM memory 44.

[0017] Although the outputs 222 and 224 are shown as dedicated outputs, a common data bus may be provided between the address decoder 22 and the sub-controllers 24, 26.

[0018] The operation of the address decoder 22 will now be described in more detail. A range of addresses is allocated to each type of memory in the memory array 4. For instance, say the total capacity of the memory array 4 is 2GB.

[0019] The addresses 0 to 16MB are allocated to the Flash memory 42 and addresses above 16MB are allocated to the SDRAM 44. This information is stored in the address decoder 22.

[0020] In use, when the processor 6 accesses the memory, for example to fetch an instruction from the Flash memory 42, the address is first passed to the memory controller 2 through the internal bus 8. When the address decoder receives a memory access request from the microprocessor 6, the address decoder 22 decodes and examines the address of the memory access request and selects the appropriate sub-controller 24, 26 on the basis of the address. If the address to be accessed is within the range of addresses allocated to the first type of memory 42, the address decoder outputs a sub-controller select signal CS1. If the address to be accessed is within the range of addresses allocated to the second type of memory 44, the address decoder outputs a sub-controller select signal CS2. The appropriate sub-controller then generates the appropriate memory access protocol signals.

[0021] In response to the sub-controller select signal CS1, the sub-controller 24 generates a plurality of memory interface signals for controlling the burst type memory 42. Figure 2 shows an example of the memory interface signals generated by the first sub-controller 24. The sub-controller 24 generates: a 22-bit address signal ADDR; a DATA signal that comprises at least one burst of 16 bits; and an address valid signal ADV. When the ADV signal is low, the address information is transmitted.

[0022] In response to the sub-controller select signal CS2, the sub-controller 26 generates a plurality of memory interface signals for controlling the SDRAM memory 44. Figure 3 shows an example of the memory interface signals generated by the second sub-controller 26. The sub-controller 26 generates: a 12 bit address signal ADDR that includes a column address COL and a row address ROW; a column address signal CAS and a row address signal RAS, which indicate when column or row data respectively is being transmitted; a DATA signal that comprises at least 16 bits; and a clock signal CLK. It will be clear to a person skilled in the art that the ROW address may be transmitted before the COL address and that the CAS and RAS signals may be active high (as shown) or active low.

[0023] The processor 6 may configure the parameters of the sub-controllers 24, 26. Examples of the sub-controller parameters that the processor may configure are the clock frequency of the memory bus, number of wait states, size of the memory type associated with the sub-controller etc. The parameters of the address decoder may also be configurable so that the address ranges allocated to each type of memory may be altered.

[0024] Figure 4 shows the pin implementation of a memory controller according to a second embodiment of the invention. In this embodiment, the memory controller is arranged to operate with three types of memory: Flash memory 42, first SDRAM 44 and second SDRAM 46. A first pin 201 outputs the first 14 bits of the address for the SDRAM memory 44 or 46 and the last 6 bits (bits 16-21) of the address for the Flash memory 42. Pin 202 outputs the 16 bit data for the SDRAM memory and the 16 bit data or the 16 MSB of the address for the Flash memory 42. Pin 203 outputs the chip select signal CS1 for the Flash memory 42. Pin 204 outputs the chip select signal CS2 for the SDRAM memory 44. Pin 205 outputs the chip select signal CS3 for the SDRAM memory 46. Pin 206 outputs a Clock Enable signal CKE1 for the Flash memory 42. Pin 207 outputs a CKE2 signal for the SDRAM memory 44. Pin 208 outputs a CKE3 signal for the SDRAM memory 46.

[0025] The memory controller may also include Read Only Memory (ROM) 29. This is used to store the code used by the device on start-up. When the microprocessor is reset (e.g. the device is switched on) the microprocessor 6 interrogates the ROM. Stored in the ROM is information regarding the type of memory to be accessed when the device is reset. For instance the ROM may include instructions that the memory controller should always access the Flash memory on reset. The

Flash memory may store information regarding the address ranges to be used by the memory controller 2. This information is read by the microprocessor and stored in the address decoder 22 of the memory controller.

[0026] The address information (i.e. ranges and type of memory) may either be hardwired into the address decoder 22 or this information may be downloaded from the boot ROM 29. Alternatively the memory controller 2 or boot ROM 29 may be programmed with instructions as to how and from where to download this information. Thus if the method for accessing the first memory can be found from the BOOT ROM/hardwired logic of the memory controller, then the device will gain access to the first memory during boot up and by downloading information from the first memory it will gain access to other memories. Altematively the device may access this information via an external interface (such as RS232) during boot up from Boot ROM 29 or the hardwired logic of memory controller 2 and by using this interface it may download information needed for accessing memories.

[0027] This way of downloading the information enables an straightforward way to change the memory components without any need to change the ASIC.

Claims

1. A memory controller for controlling the transfer of data to and from a memory array, wherein the memory array includes a first type of memory and a second type of memory, the first type having a different signalling protocol from the second type of memory, wherein the memory controller comprises:

   an address decoder having an input for receiving a memory access request, said memory access request including the address of the memory array to be accessed, and an output for outputting the address of the memory array to be accessed;
   a first sub-controller for generating a plurality of memory interface signals for controlling the first type of memory, said first sub-controller being operated in response to addresses within a first range of addresses output by the address decoder; and
   a second sub-controller for generating a plurality of memory interface signals for controlling the second type of memory, said second sub-controller being operated in response to addresses within a second, non-overlapping range of addresses output by the address decoder.

2. A memory controller according to claim 1 wherein the first type of memory is a burst mode type of memory.

3. A memory controller according to claim 2 wherein the first type of memory is flash memory.

4. A memory controller according to claim 1, 2 or 3 wherein the first type of memory is MROM.

5. A memory controller according to any preceding claim wherein the second type of memory is Synchronous Dynamic Random Access Memory.

6. A memory controller according to any preceding claim 1, 2 or 3 wherein parameters of the memory controller are configurable.

7. A memory controller according to claim 6 wherein the first and second range of addresses are configurable.

8. An electronic device including a memory controller as claimed in any of claims 1 to 7.

9. An electronic telecommunications device including a memory controller as claimed in any of claims 1 to 7.

10. A method of controlling the transfer of data to and from a memory array in an electronic device, wherein the memory array includes a first type of memory and a second type of memory, the first type having a different signalling protocol from the second type of memory, wherein the method comprises:

    receiving a memory access request, said memory access request including the address of the memory array to be accessed, and outputting the address of the memory array to be accessed;
    in response to addresses within a first range of addresses generating a plurality of memory interface signals for controlling the first type of memory; and
    in response to addresses within a second, non-overlapping range of addresses generating a plurality of memory interface signals for controlling the second type of memory.

11. A memory controller substantially as described herein with reference to the accompanying drawings.

12. A method of controlling memory accesses substantially as described herein with reference to the accompanying drawings.

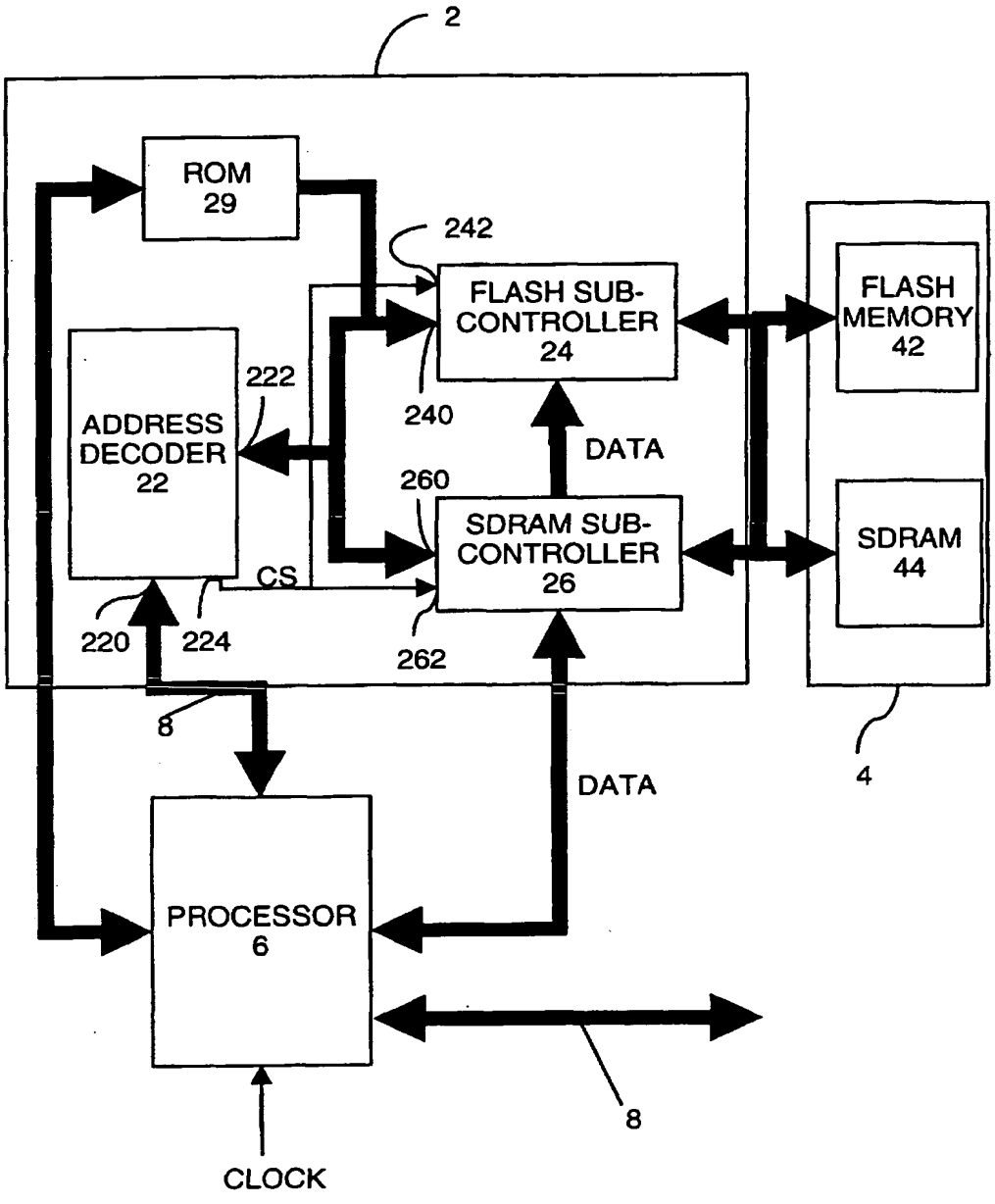

2
ROM
29
242
FLASH SUB-
CONTROLLER
24
FLASH
MEMORY
42
ADDRESS
DECODER
22
222
240
DATA
260
SDRAM SUB-
CONTROLLER
26
SDRAM
44
CS
220
224
262
8
DATA
4
PROCESSOR
6
8
CLOCK

Fig. 1

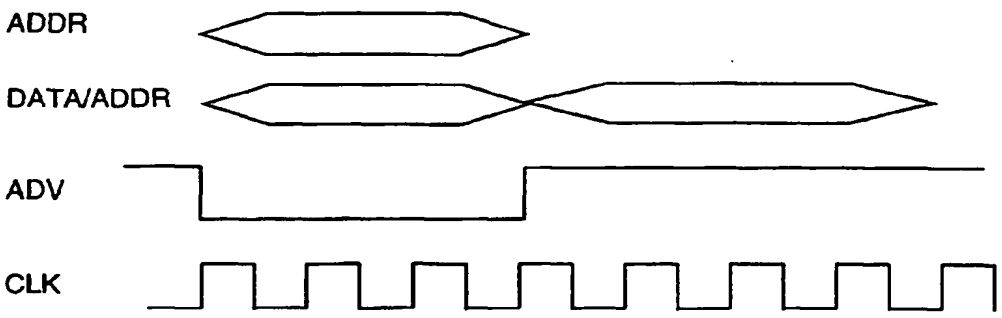


Fig. 2

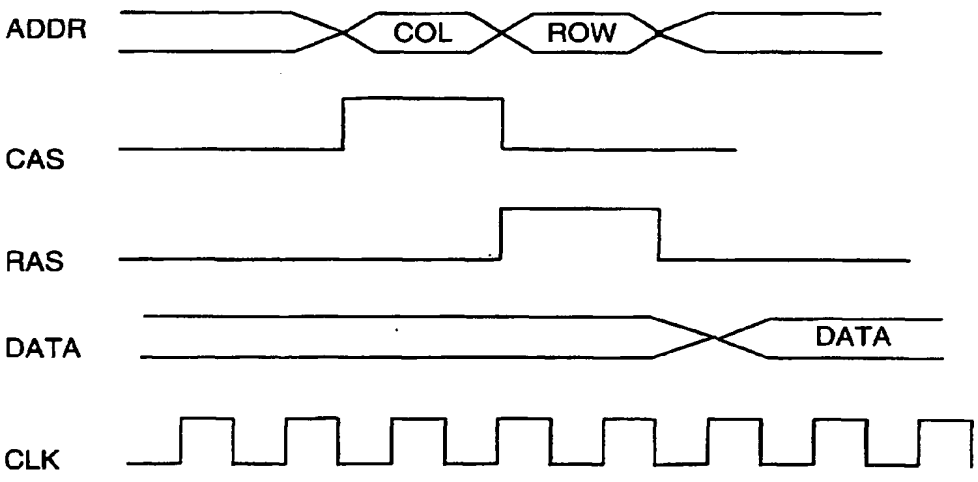
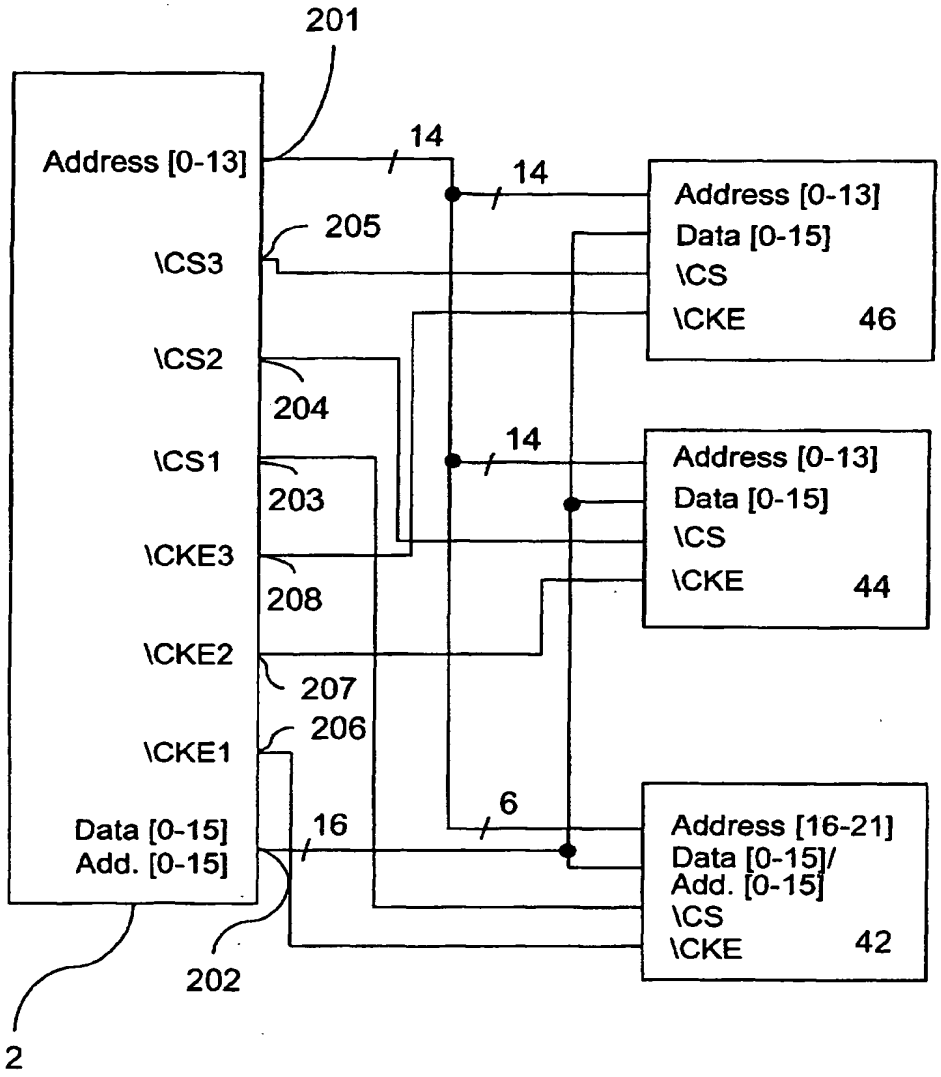


Fig. 3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14
14
Address [0-13]
Data [0-15]
\CS
\CKE
46
205
\CS3
\CS2
204
\CS1
203
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Address [0-13]
Data [0-15]
\CS
\CKE
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\CKE3
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\CKE2
207
206
\CKE1
6
16
Data [0-15]
Add. [0-15]
Address [16-21]
Data [0-15]/
Add. [0-15]
\CS
\CKE
42
202
2

Fig. 4